

### Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

### Listing of Claims:

1           1.   (currently amended) A finite impulse response filter  
2 cell, having at least three inputs and at least two outputs,  
3 the finite impulse response filter cell coupled to receive a  
4 clocking signal, comprising:  
5           a multiplexer having at least two multiplexer inputs and  
6 an output, the multiplexer operable at substantially half the  
7 clocking signal rate, each of the at least two multiplexer  
8 inputs coupled to one of the at least three inputs of the  
9 finite impulse response filter cell;  
10          a multiplier including an output and at least two  
11 multiplier inputs, the first multiplier input receiving a  
12 coefficient signal representing a FIR coefficient, the second  
13 multiplier input coupled to one of the at least three inputs  
14 of the finite impulse response filter cell;  
15          a summer having at least two summer inputs and an output,  
16 the first and second summer inputs coupled to receive the  
17 multiplexer output and the multiplier output; [and]  
18          at least two slave sample and hold circuits each having a  
19 slave input and a slave output, the at least two slave inputs  
20 of the plurality coupled to the summer output, the at least  
21 two slave outputs couple to form the at least two outputs of  
22 the finite impulse response filter cell, each slave sample and

23 hold circuit operable at substantially half the clocking  
24 signal rate; and

25 a conversion circuitry coupled to the second multiplier  
26 input, the conversion circuitry operable to convert a digital  
27 value at the second multiplier input into an analog signal.

1 2. (original) The finite impulse response filter of  
2 claim 1, wherein each coefficient signal comprises a digital  
3 value.

1 3. (canceled)

1 4. (currently amended) A finite impulse response filter  
2 cell, having at least two inputs and an output, the finite  
3 impulse response filter cell coupled to receive a clocking  
4 signal, comprising:

5 a multiplier including an output and at least two  
6 multiplier inputs, the first multiplier input receiving a  
7 coefficient signal representing a FIR coefficient, the second  
8 multiplier input coupled to one of the at least two inputs of  
9 the finite impulse response filter cell;

10 a summer having at least two summer inputs and an output,  
11 the first summer input coupled to receive the multiplier  
12 output, the second summer input coupled to one of the at least  
13 two inputs of the finite impulse response filter cell;

14 at least two slave sample and hold circuits each having a  
15 slave input and a slave output, the at least two slave inputs  
16 coupled to the summer output, each slave sample and hold  
17 circuit operable at half the clocking signal rate; [and]

18 a multiplexer having at least two multiplexer inputs and  
19 an output, each of the at least two slave outputs coupled to  
20 one of the at least two multiplexer inputs, the multiplexer  
21 operable at half the clocking signal rate, the multiplexer

22 output couples to form the output of the finite impulse  
23 response filter cell; and  
24 a conversion circuitry coupled to the second multiplier  
25 input, the conversion circuitry operable to convert a digital  
26 value at the second multiplier input into an analog signal.

1 5. (original) The finite impulse response filter of  
2 claim 4, wherein each coefficient signal comprises a digital  
3 value.

1 6. (canceled)

1 7. (original) A finite impulse response filter having  
2 an input and an output, comprising:  
3 a master sample and hold circuit including a master  
4 input and a master output, the master input coupled to form  
5 the input of the finite impulse response filter, the master  
6 sample and hold circuit operable to sample a first input  
7 signal and hold the value of the first input signal on the  
8 master output for a first predetermined period of time, the  
9 master sample and hold circuit operable at a clock speed;  
10 at least two slave sample and hold circuits, each of  
11 the at least two slave sample and hold circuits comprising a  
12 slave input and a slave output, each the at least two slave  
13 inputs coupled to the master output, each of the at least two  
14 sample and hold circuits operable to sample the master output  
15 signal and hold the value of the signal on the plurality of  
16 slave outputs for a second predetermined period of time, the  
17 at least two slave sample and hold circuits operable at  
18 substantially  $1/k$  times the clock speed of the master sample  
19 and hold circuit, where  $k$  equals the number of slave sample  
20 and hold circuits;

21           a first multiplexer, having at least two first  
22 multiplexer inputs and a first multiplexer output, each of the  
23 at least two first multiplexer inputs coupled to one of the at  
24 least two slave outputs, the first multiplexer operable at  
25 substantially  $1/k$  times the clock speed of the master sample  
26 and hold circuit; and  
27           at least one tap block having a tap block input and  
28 a tap block output, the tap block input coupled to the first  
29 multiplexer output, the at least one tap block, comprising,  
30           a multiplier having a first and a second multiplier  
31 input and an multiplier output, the first multiplier input  
32 coupled to the tap block input, the second multiplier input  
33 coupled to receive a coefficient signal representing a FIR  
34 coefficient,  
35           a summer including an output and a first and a  
36 second summer input, the first input coupled to the multiplier  
37 output,  
38           at least two slave sample and hold circuits, each of  
39 the at least two slave sample and hold circuits comprising a  
40 slave input and a slave output, each the at least two slave  
41 inputs coupled to the summer output, the at least two slave  
42 sample and hold circuits operable at substantially  $1/k$  times  
43 the clock speed of the master sample and hold circuit, where  $k$   
44 equals the number of slave sample and hold circuits,  
45           a second multiplexer, having at least two second  
46 multiplexer inputs and a second multiplexer output, each of  
47 the at least two second multiplexer inputs coupled to one of  
48 the at least two slave outputs of the tap block, the second  
49 multiplexer operable at substantially  $1/k$  times the clock  
50 speed of the master sample and hold circuit, the second  
51 multiplexer output coupled to form the tap block output, the  
52 tap block output couples to form a filter output.

1        8.    (original) The finite impulse response filter of  
2 claim 7, wherein each coefficient signal comprises a digital  
3 value.

1        9.    (original) The finite impulse response filter of  
2 claim 7, further comprises a conversion circuitry coupled to  
3 the second multiplier input, the conversion circuitry operable  
4 to convert a digital value at the second multiplier input into  
5 an analog signal.

1        10.   (original) An finite impulse response filter having  
2 an output, comprising:

3            a master sample and hold circuit including a master  
4 input and a master output, the master input coupled to the  
5 input of the finite impulse response filter, the master sample  
6 and hold circuit operable to sample a first input signal and  
7 hold the value of the first input signal on the master output  
8 for a first predetermined period of time, the master sample  
9 and hold circuit operable at a clock speed;

10           a plurality of slave sample and hold circuits, each  
11 of the plurality of slave sample and hold circuits comprising  
12 a slave input and a slave output, each of the plurality of  
13 sample and hold circuits operable to sample a signal and hold  
14 the value of the signal on the plurality of slave outputs for  
15 a second predetermined period of time, the plurality of slave  
16 sample and hold circuits operable at substantially half the  
17 clock speed of the master sample and hold circuit;

18           a first pair of the plurality of slave sample and  
19 hold circuits having each slave input directly connected to  
20 the master output;

21           a plurality of multiplexers, each comprising at  
22 least a first and second multiplexer input and an multiplexer  
23 output, the first multiplexer operable at substantially half

24 times the clock speed of the master sample and hold circuit,  
25 each first and second multiplexer inputs coupled to one pair  
26 of slave outputs;

27 a plurality of multipliers, each of the plurality of  
28 multipliers including an output and a first and a second  
29 multiplier input, each first multiplier input receiving a  
30 coefficient signal representing a FIR coefficient, each second  
31 multiplier input coupled to the output of the first  
32 multiplexer of the plurality of multiplexers; and

33 a plurality of summers, each of the summers  
34 including an output and a first and a second summer input,  
35 each first summer input coupled to one of the plurality of  
36 multiplier outputs, the second summer input of the first  
37 summer couples to ground, each remaining second summer inputs  
38 coupled to one of the plurality of multiplexer outputs, each  
39 pair of slave inputs succeeding the first pair of slave inputs  
40 connected to one of the plurality of summer outputs;

41 the number of plurality of slave sample and hold  
42 circuits equals  $2N$ , the number of plurality of multiplexers  
43 equals  $N$ , the number of plurality of summers equals  $N$ , the  
44 number of plurality of multipliers  $N+2$ ;

45 the multiplexer output of the last one of the  
46 plurality of multiplexers couples to form the output of the  
47 finite impulse response filter.

1 11. (original) The finite impulse response filter of  
2 claim 10, wherein each coefficient signal comprises a digital  
3 value.

1 12. (original) The finite impulse response filter of  
2 claim 10, further comprises a conversion circuitry coupled to  
3 the second multiplier input, the conversion circuitry operable

4 to convert a digital value at the second multiplier input into  
5 an analog signal.

1 13. (original) A method of making an finite impulse  
2 response filter which has an output, comprising the steps of:  
3 coupling an input signal to a master input of a  
4 master sample and hold circuit;  
5 directly connecting a master output of the master  
6 sample and hold circuit to a plurality of slave sample and  
7 hold circuits;  
8 multiplexing the plurality of slave sample and hold  
9 circuit output signals;  
10 directly connecting the multiplexed output to at  
11 least one tap block cell having a first and second input and  
12 an output, including a multiplier, a summer, a plurality of  
13 slave sample and hold circuits and a multiplexer;  
14 supplying a fixed tap coefficient signal to an input  
15 of the multiplier;  
16 multiplying the first input of the tap block cell  
17 and the fixed tap coefficient signal;  
18 summing an output of the multiplier with the second  
19 input of the tap block cell;  
20 connecting an output of the summer to the inputs of  
21 the plurality of slave sample and hold inputs of the tap block  
22 cell;  
23 connecting the slave outputs of the plurality of  
24 slave sample and hold circuits to the plurality of multiplexer  
25 inputs of the multiplexer in the tap block; and  
26 multiplexing the slave output signals to generate  
27 the finite impulse response filter output.

1 14. (original) The method of claim 13, wherein the first  
2 input of the first tap block cell is grounded.